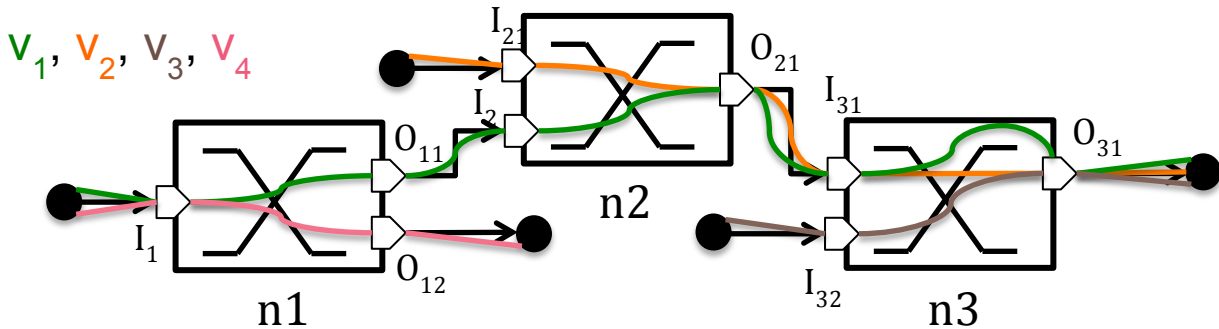


ARINC664 – AFDX networks

Given the network architecture depicted below, compute the worst-case end-to-end latency of flow v_1 : W_1^{n3} .

The timing parameters are given hereafter, using the same notation as in the lecture slides.



$sl = 3$ (switch technological latency)

$C_i = 1$, for all i (worst case transmission delay)

$P_1 = P_3 = P_4 > P_2$ (flows priority)

$T_1 = 10$ (period of flow v_1)

$T_2 = T_3 = T_4 = 5$ (periods of flows v_2, v_3, v_4)

$Path_1 = \{ES_1, O_{11}, O_{21}, O_{31}\}$

Formulas:

$$W_{i,t}^{last_i} = X_{i,t} + \delta_i + (|Path_i| - 1) \cdot sl$$

$$\delta_i = \sum_{p \in Path_i} 1_{p,i} \cdot \max(C_j)$$

$$\begin{aligned}
X_{i,t} \leq & \sum_{\substack{v_j \in hp_i \\ Path_i \cap Path_j \neq \emptyset}} \left(1 + \left\lfloor \frac{W_{i,t}^{last_i} + B_{i,j}}{T_j} \right\rfloor \right)^+ \cdot C_j \\
& + \sum_{\substack{v_j \in sp_i \cup \{v_i\} \\ Path_i \cap Path_j \neq \emptyset}} \left(1 + \left\lfloor \frac{t + A_{i,j}}{T_j} \right\rfloor \right)^+ \cdot C_j \\
& + \sum_{h \in Path_i} \left(\max_{\substack{v_j \in hp_i \cup sp_i \cup \{v_i\} \\ h \in Path_j}} (C_j) \right) \\
& - C_i
\end{aligned}$$

$$A_{i,j} = S_{max_i}^{first_{i,j}} - S_{min_j}^{first_{i,j}} + S_{max_j}^{first_{i,j}} - M_i^{first_{i,j}}$$

$$B_{i,j} = -S_{min_j}^{last_{i,j}} + S_{max_j}^{first_{i,j}} - M_i^{first_{i,j}}$$

$$M_i^h = \sum_{k=first_i}^{h-1} (sl + \min_{\substack{j \in [1,n] \\ k \in Path_j}} (\frac{Lmin_j}{R}))$$

$$BP_i^{m+1} = \sum_{\substack{j \in [1,n] \\ Path_i \cap Path_j \neq \emptyset}} \left\lfloor \frac{BP_i^m}{T_j} \right\rfloor \cdot C_j$$